EE 330 Spring 2024 Rm 1011 Coover

Weeks

8:50-9:40

ROW	8	7	6	5	4	3	2	1
6								
5						Spencer Rudin	Ibram Shenouda	Zachary Sears
4	Zane Cozart	Sean O'Brien	Nathan Cook	Rakesh Varma	Clayton Kramper	Eddy Andrade	Christopher Penne	Ryan Ellerbach
3	Elias Colsch	Jonathan Wetenkamp	Yash Gaonkar	Aden Harriman	Peter Dea	Mackenzie Ray	Olivia Price	Maheeka Devarakonda
2	Mason Suarez	Emerson Hollar	Alex Crandall	Konnor Kivimagi	Cayden Kelley	Cade Kuennen	Sam Burns	Sean Douglas
1	Jackson Phillips	Vrba Isaac	Luke Post	Bennet Palkovic	Zach O'Brien	Huyen Vy Pham	James Mendenhall	Cole Dustin

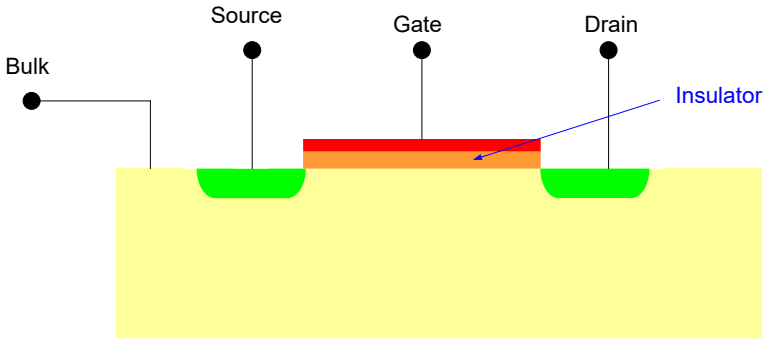
EE 330
Lecture 7

Propagation Delay

Review from Last Time

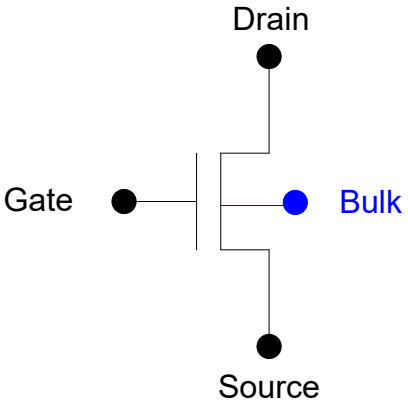
MOS Transistor

Qualitative Discussion of n-channel Operation

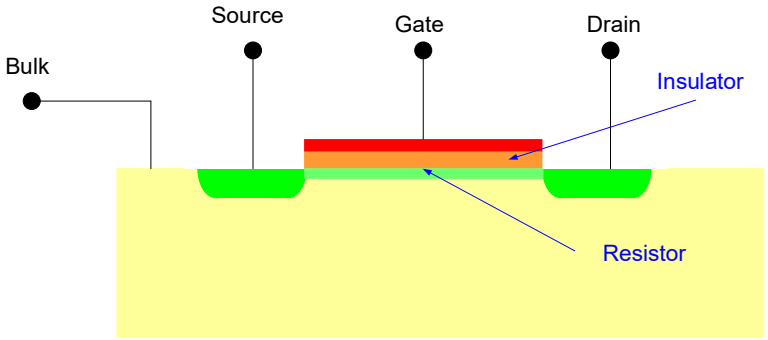


n-channel MOSFET

For V_{GS} small



MOSFET actually 4-terminal device



n-channel MOSFET

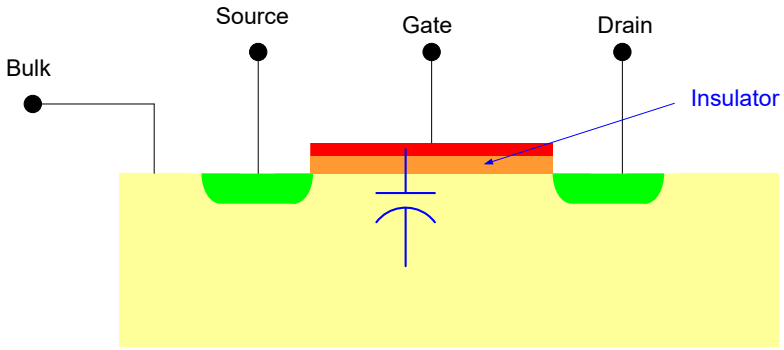
For V_{GS} large

- Region under gate termed the “channel”
- When “resistor” is electrically created, region where it resides in channel is termed an “inversion region”

Review from Last Time

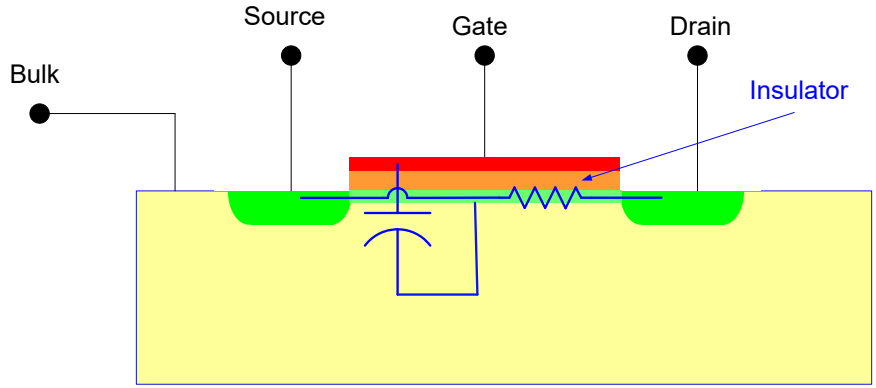
MOS Transistor

Qualitative Discussion of n-channel Operation

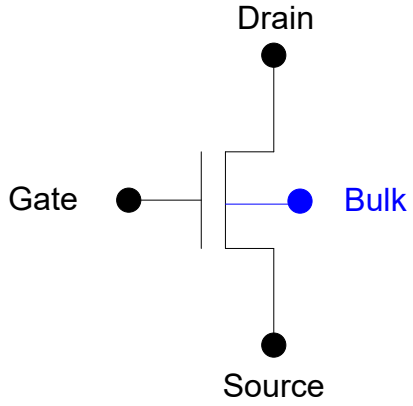


n-channel MOSFET

For V_{GS} small



n-channel MOSFET



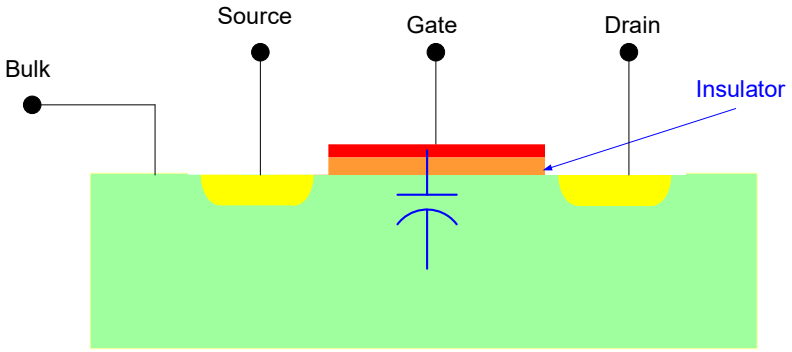
For V_{GS} large

- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

Review from Last Time

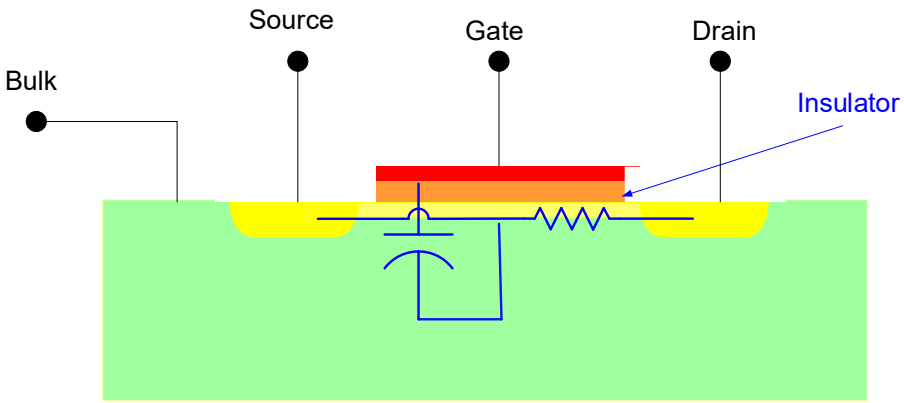
MOS Transistor

Qualitative Discussion of p-channel Operation

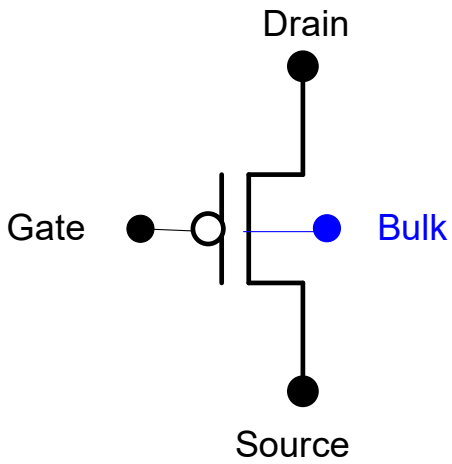


p-channel MOSFET

For $|V_{GS}|$ small



p-channel MOSFET

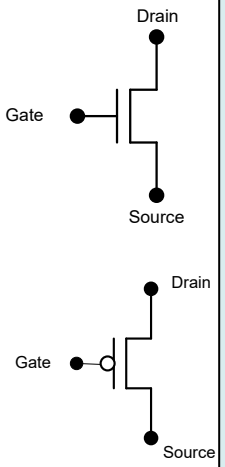


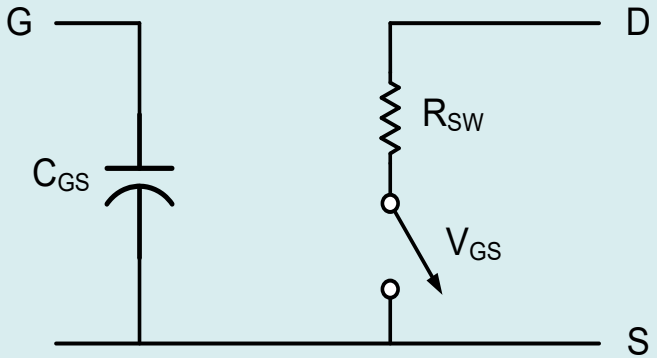
For $|V_{GS}|$ large

- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

Review from Last Time

Improved Switch-Level Model





Switch closed for $|V_{GS}|$ large

Alt: If S near V_{DD} for p-ch and S near gnd for n-ch and where A denotes Boolean signal on Gate

Switch closed for A =1 , n-ch
Switch closed for A =0 , p-ch

Switch-level model including gate capacitance and channel resistance

C_{GS} and R_{SW} dependent upon device sizes and process

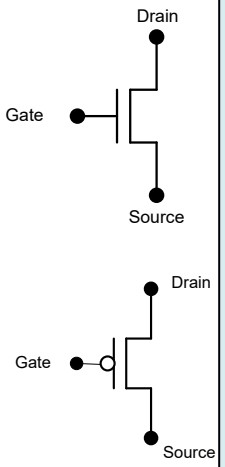
For minimum-sized devices in a 0.5u process with V_{DD}=5V

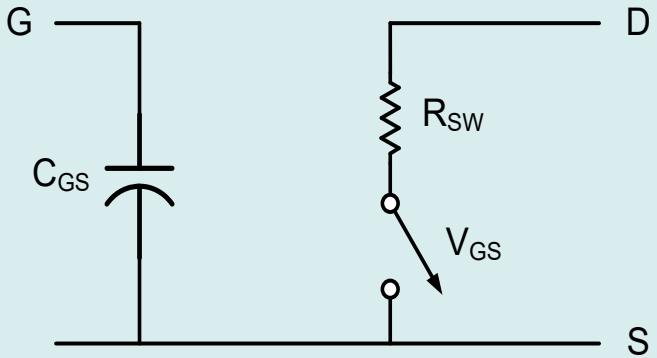
$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \ \ n-channel \\ 6K\Omega \ \ p-channel \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Review from Last Time

Improved Switch-Level Model





Switch closed for $|V_{GS}|$ large

Alt: If S near V_{DD} for p-ch and S near gnd for n-ch and where A denotes Boolean signal on Gate

Switch closed for A =1 , n-ch
Switch closed for A =0 , p-ch

Switch-level model including gate capacitance and channel resistance

C_{GS} and R_{SW} dependent upon device sizes and process

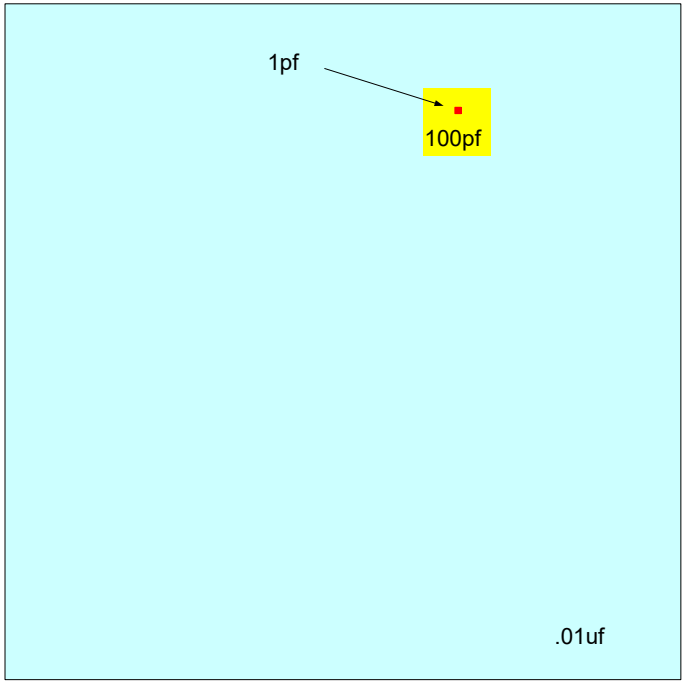
Will assume for minimum-sized devices in a 0.18u process with V_{DD}=2V

$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw}} \cong \begin{cases} \mathbf{2K\Omega \ \ n-channel} \\ \mathbf{6K\Omega \ \ p-channel} \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Review from Last Time

Is a capacitor of 1.5fF small enough to be neglected?



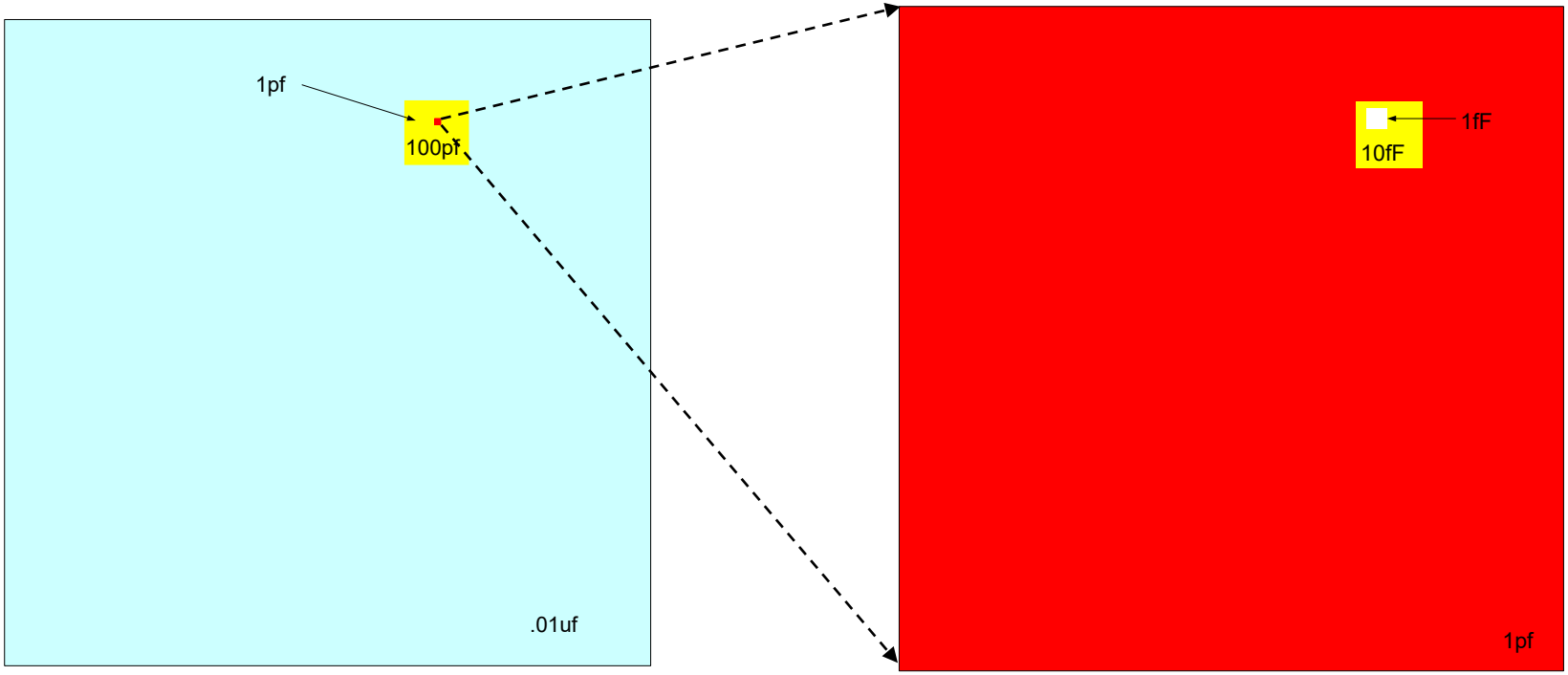
From EE 201 Parts Kit

Capacitors (Farads)		
100p	3	
470p	3	
0.001u	3	2
0.0047u	3	2
0.01u	3	
0.047u	3	
0.1u	3	1
0.47u	3	
1u	3	
10u	3	
100u	3	

Area allocations shown to relative scale:

Review from Last Time

Is a capacitor of 1.5fF small enough to be neglected?

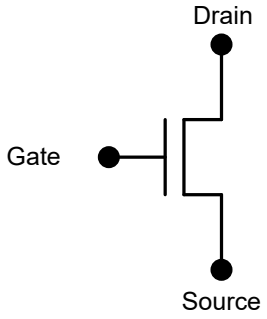


Area allocations shown to relative scale:

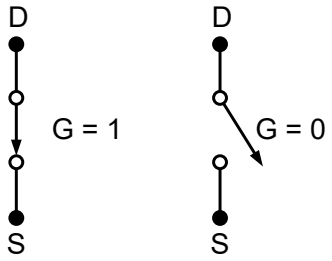
- **Not enough information at this point to determine whether this very small capacitance can be neglected**
- **Will answer this important question later**

Review from Last Time

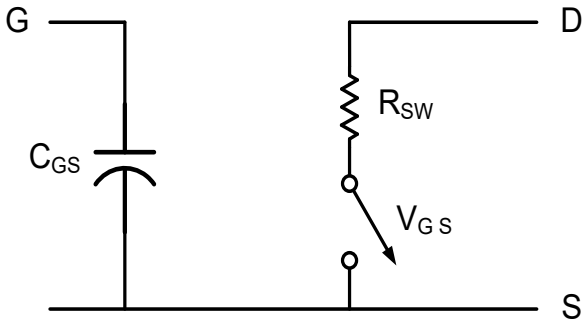
Model Summary (for n-channel)



1. Switch-Level model



2. Improved switch-level model



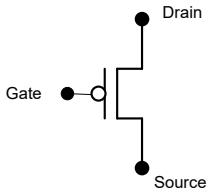
Switch closed for V_{GS}= large

Switch open for V_{GS}= small

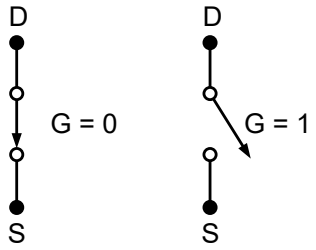
Other models will be developed later

Review from Last Time

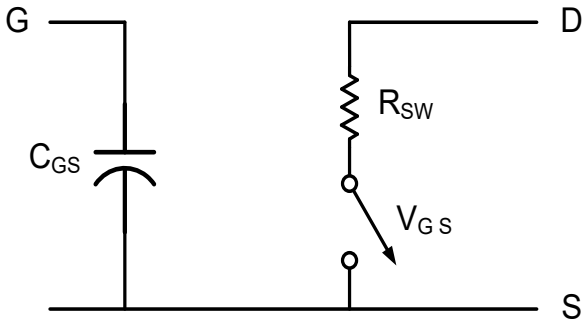
Model Summary (for p-channel)



1. Switch-Level model



2. Improved switch-level model



Switch closed for $|V_{GS}|$= large

Switch open for $|V_{GS}|$= small

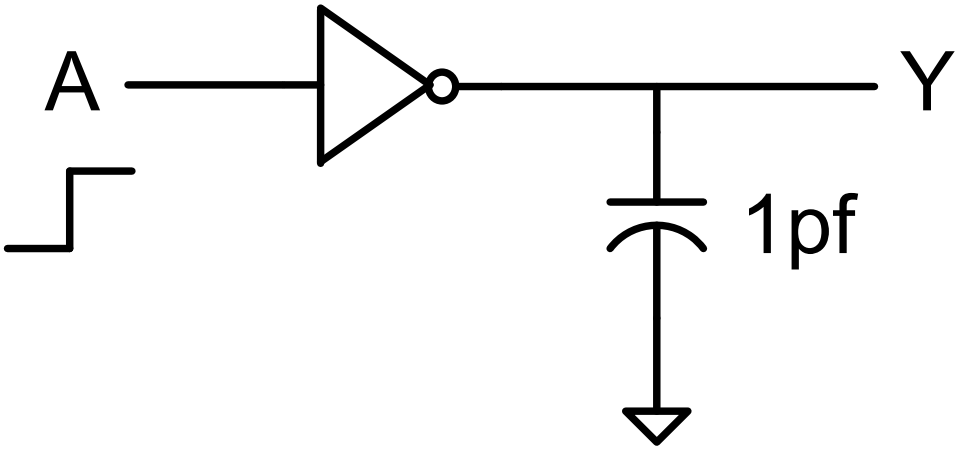
Other models will be developed later

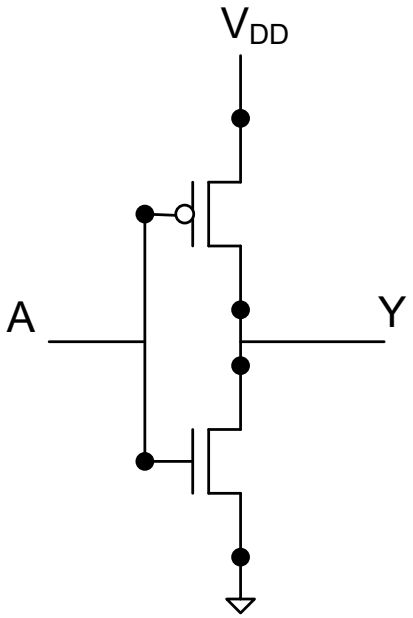
Propagation Delay

Example

What are t_{HL} and t_{LH}?

Assume V_{DD}=5V



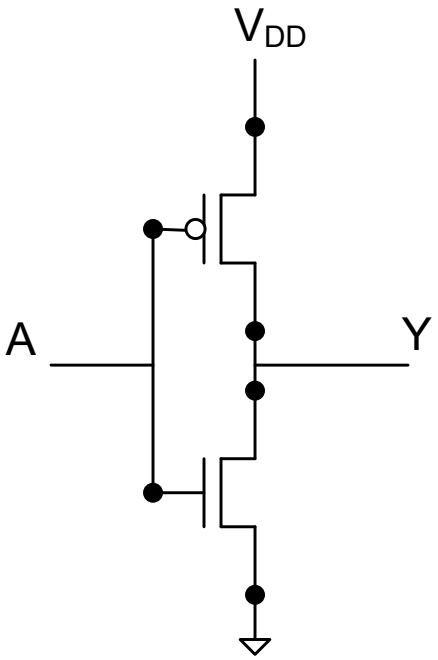


Inverter

With basic switch level model ?

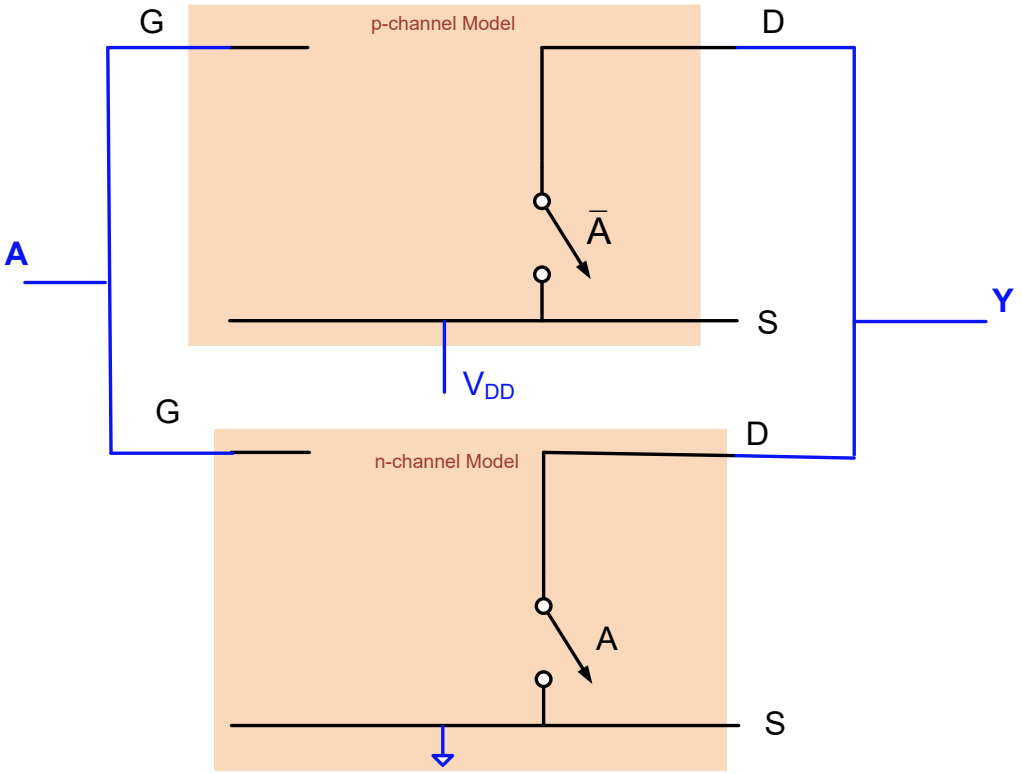
With improved switch level model ?

Example



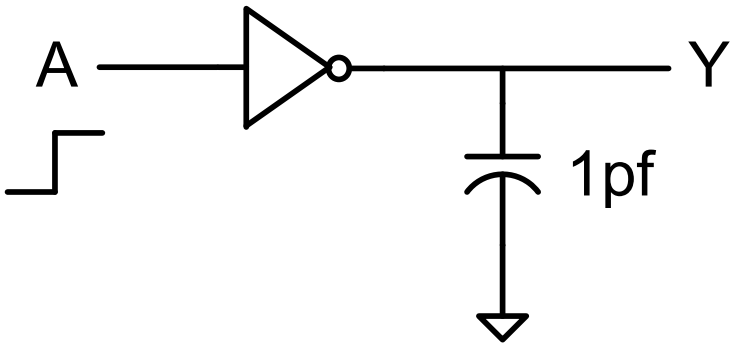
Inverter

Inverter with basic switch-level model

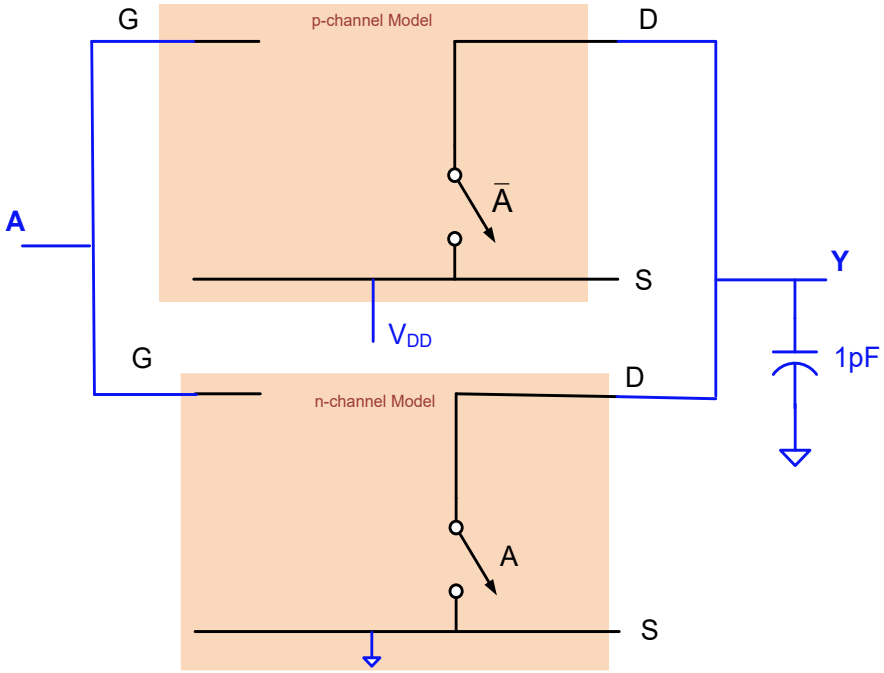


Example

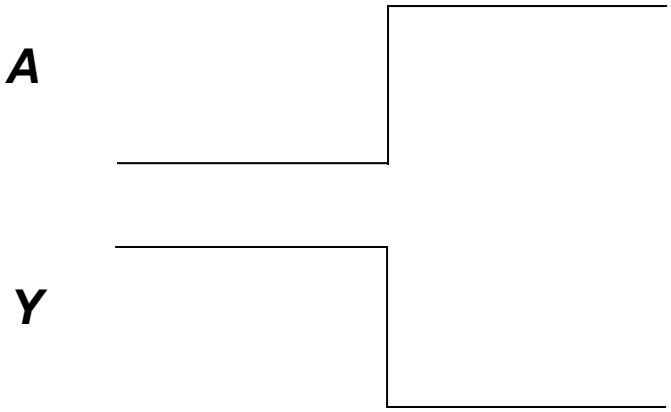
What are t_{HL} and t_{LH} at output?



Assume ideal step at A input



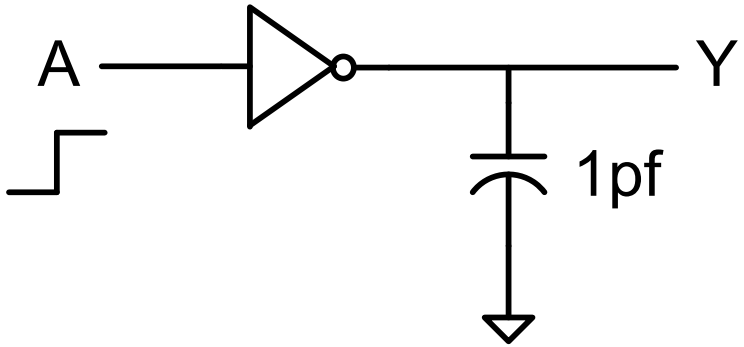
With basic switch level model



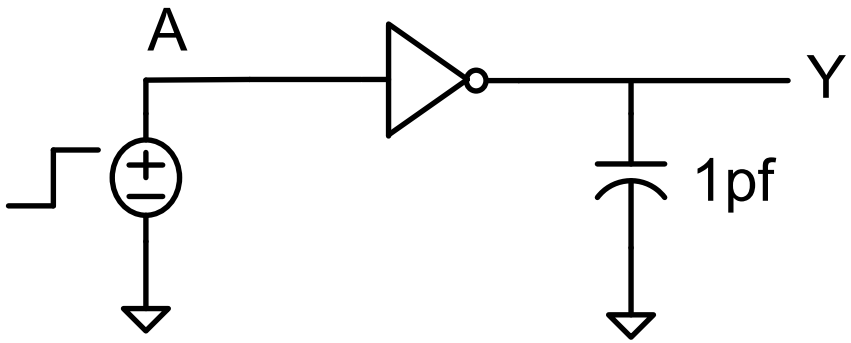
$t_{HL}=t_{LH}=0$

Example (cont)

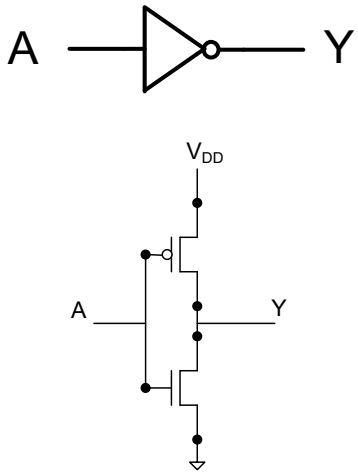
With simple switch-level model $t_{HL}=t_{LH}=0$



With improved model ?



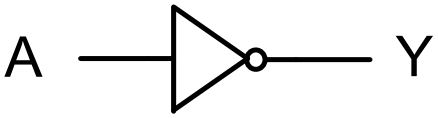
Inverter Model?

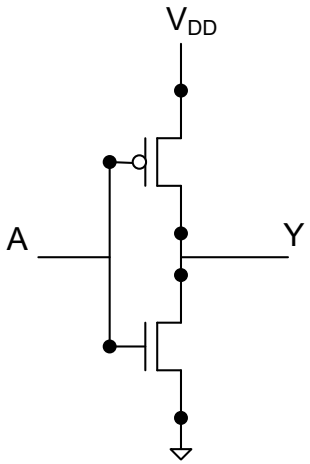


Example (cont)

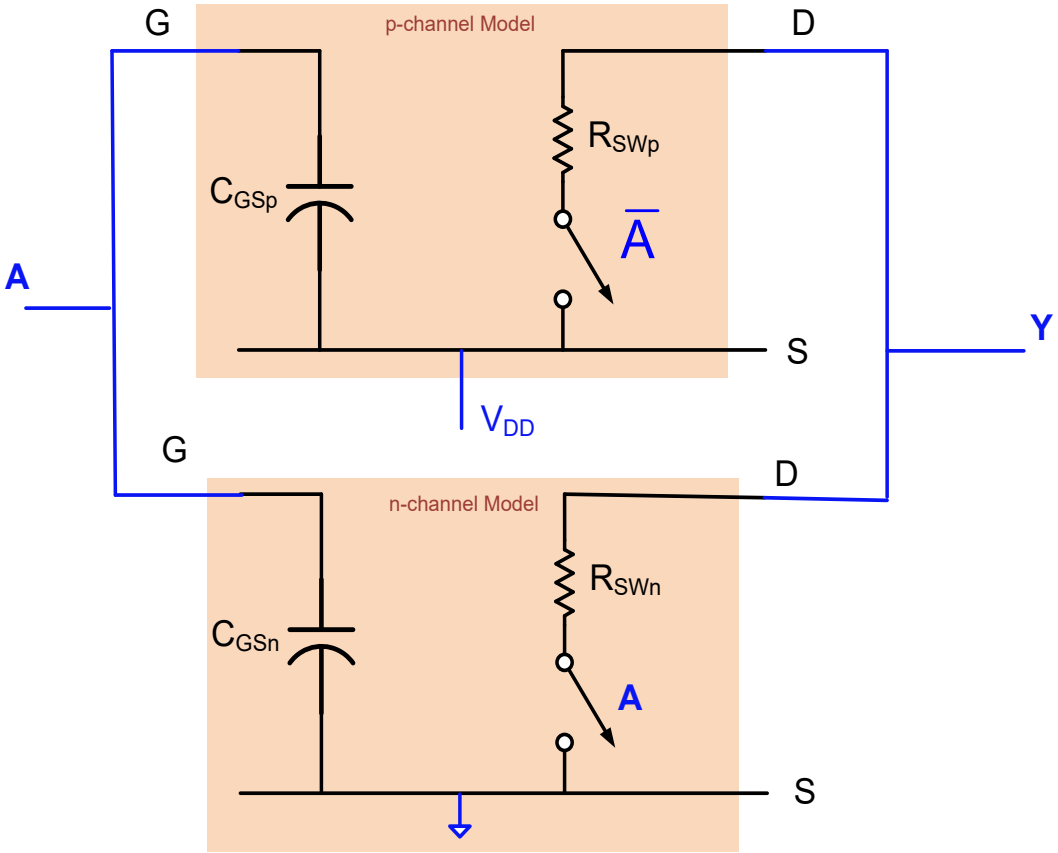
Inverter with improved model

Inverter Model



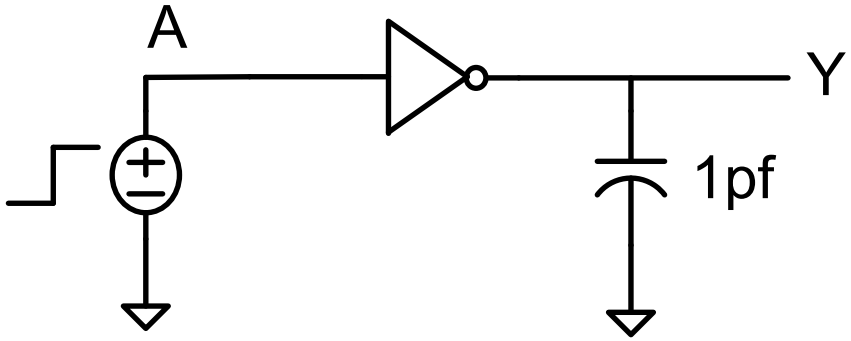


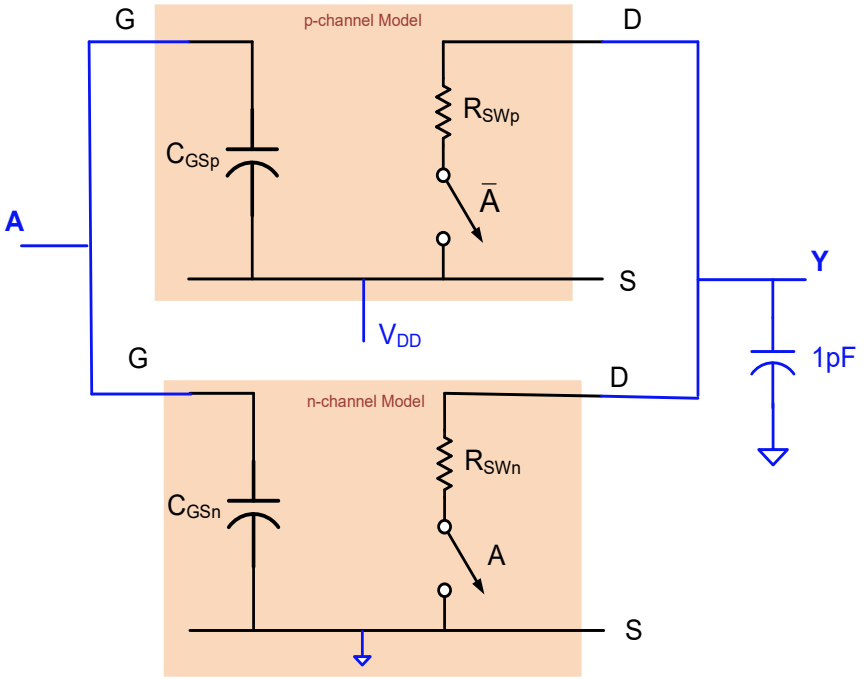
Inverter with Improved Model



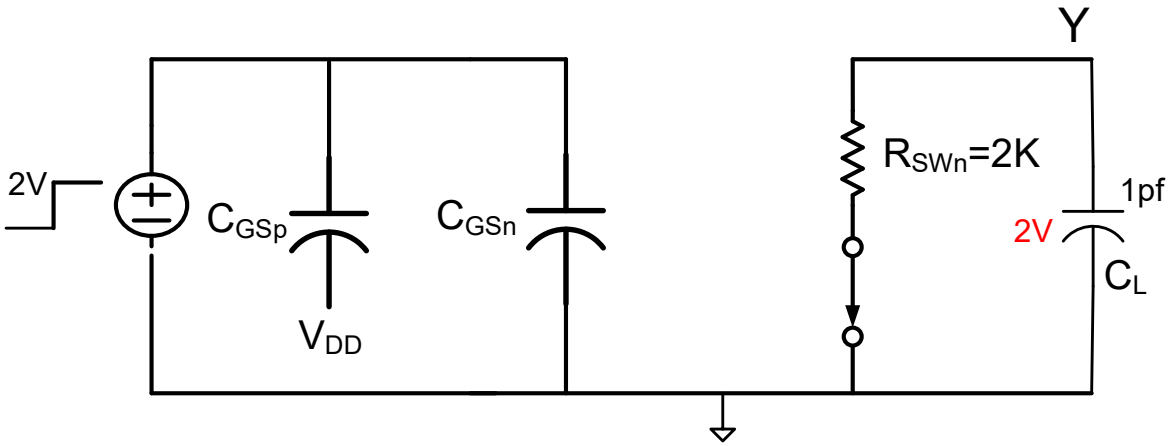
Example (cont)

With improved model $t_{HL}=?$





To initiate a HL output transition, assume Y has been in the high state for a long time, lower switch closes at time t=0, and upper switch opens just prior to t=0

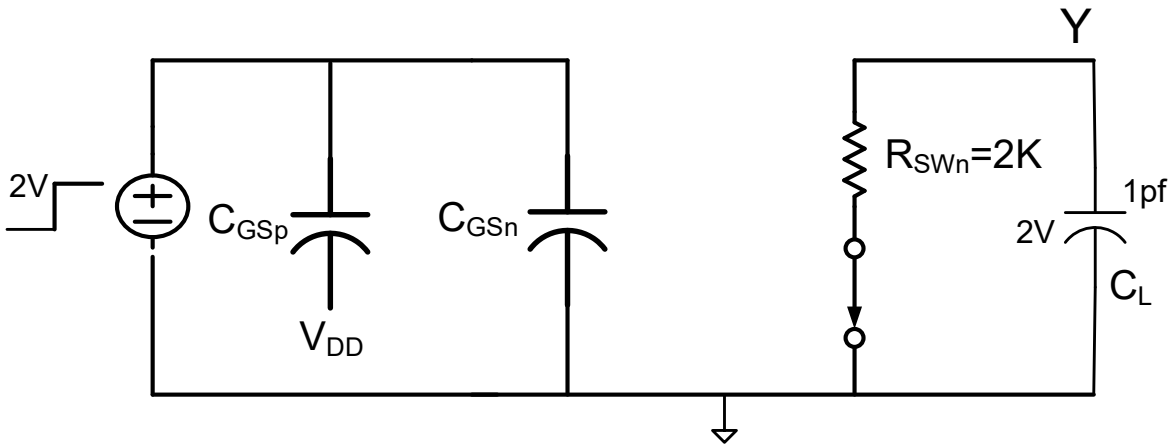


2V is the initial condition on C_L

Example (cont)

With improved model

t_{HL}=?



Recognize circuit (specifically on right) as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

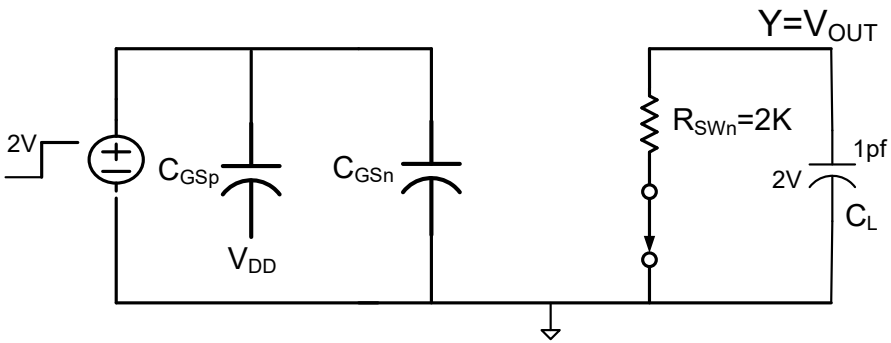
where F is the final value, I is the initial value and τ is the time constant of the circuit

(from Chapter 7 of Nilsson and Riedel)

For the circuit above, F=0, I=2 and $\tau = R_{SWn}C_L$

Example (cont)

With improved model

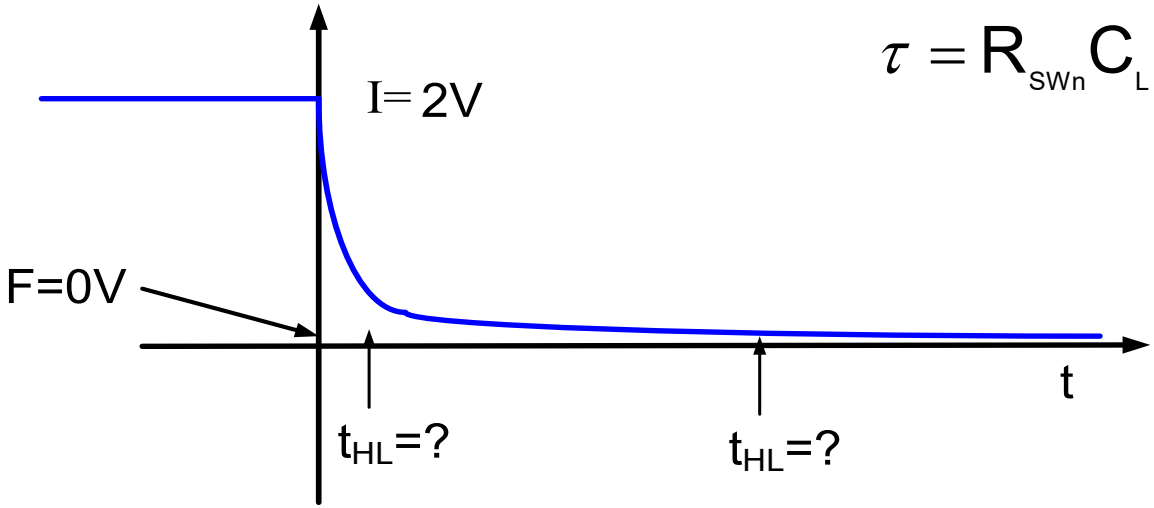


$t_{HL}=?$

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 2e^{-\frac{t}{\tau}}$$

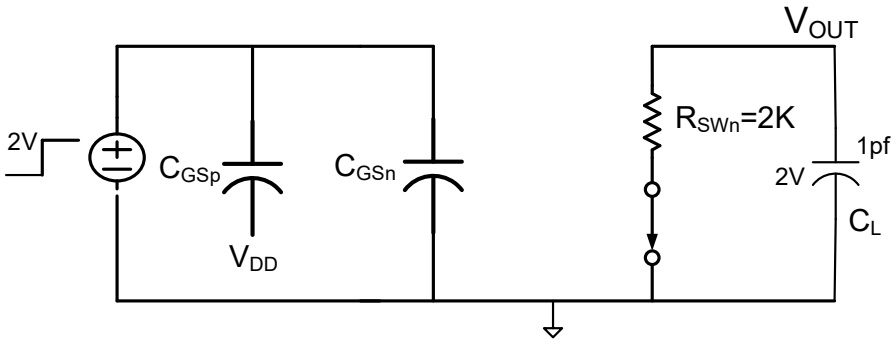
$$\tau = R_{SWn}C_L$$

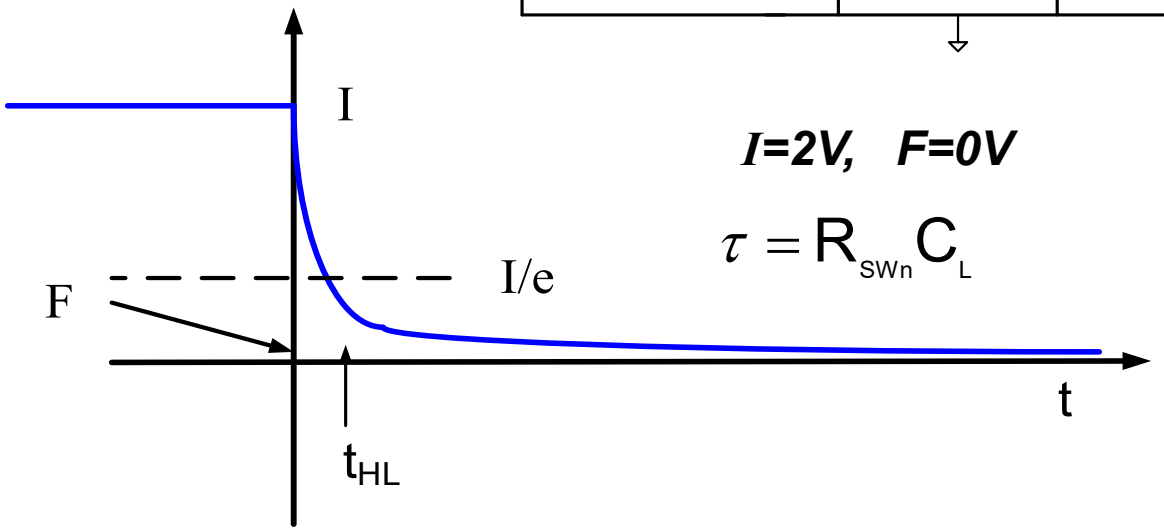


how is t_{HL} defined?

Example (cont)

t_{HL}=?





I=2V, F=0V

$$\tau = R_{SWn} C_L$$

Define t_{HL} to be the time taken for output to drop to I/e

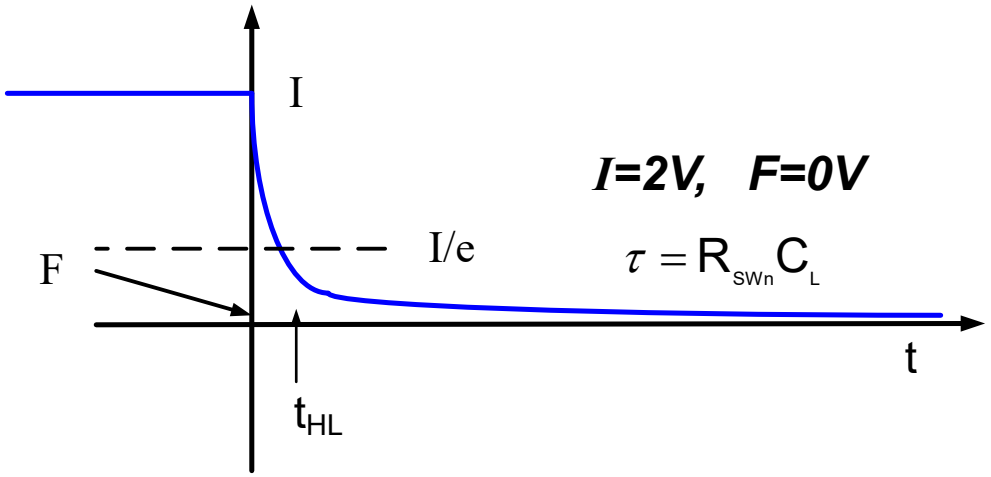
$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Longrightarrow \quad \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

Is this simply a mathematical definition or does it have some practical significance?

t_{HL} as defined here and as verified by experimental verification has proven useful at analytically predicting response time of circuits

Example (cont)

With improved model



$$\frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

$$\frac{I}{e} = Ie^{-\frac{t_{HL}}{\tau}}$$

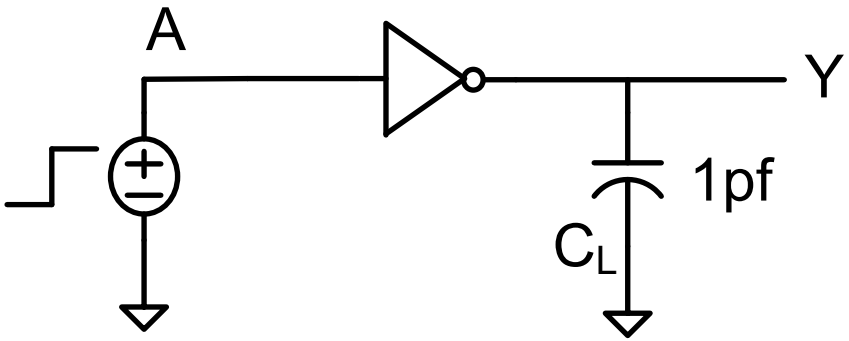
$$\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}$$

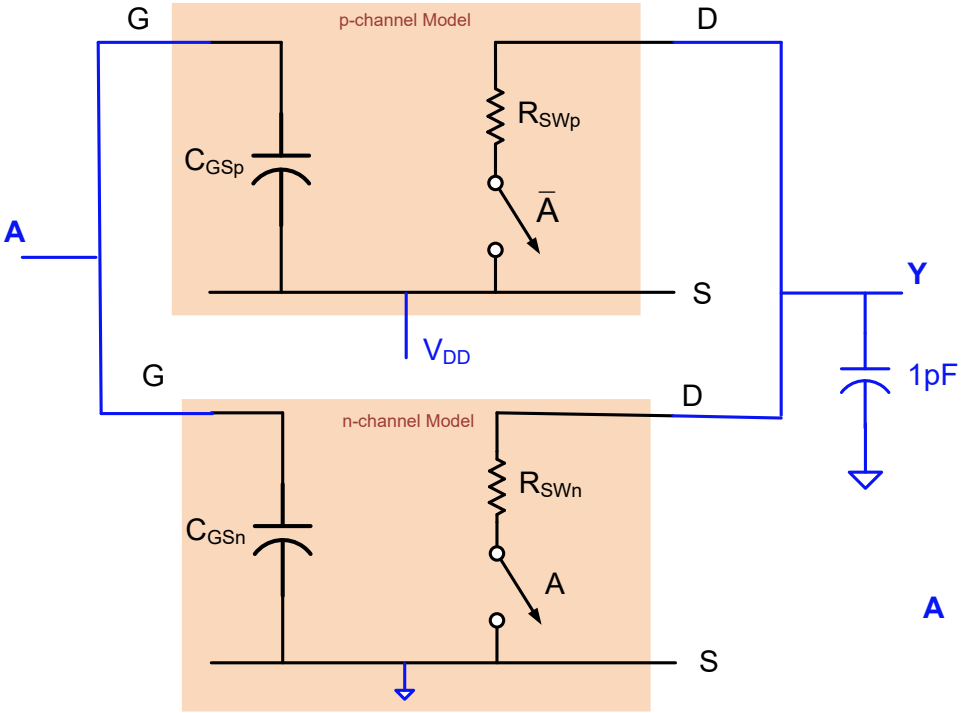
$$t_{HL} = \tau \quad \Rightarrow \quad t_{HL} = R_{SWn} C_L$$

Both experimental results and accurate computer simulations show that this reasonably accurately predicts how quickly following stages recognize that a logic transition has taken place !!

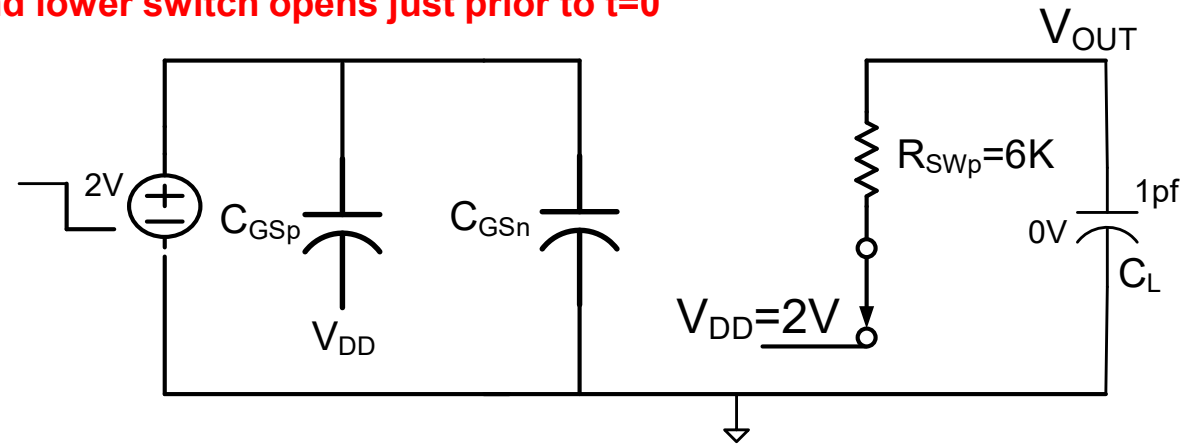
Example (cont)

With improved model $t_{LH}=?$





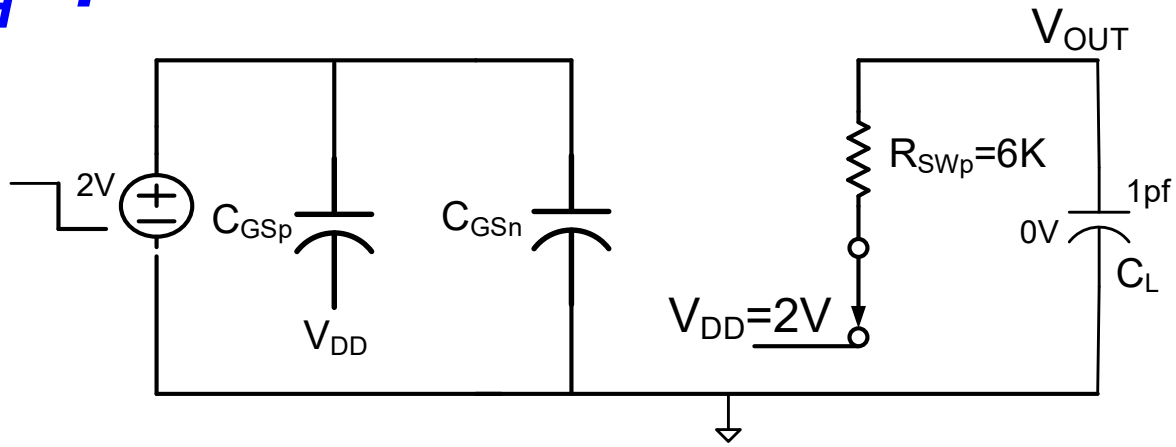
Assume output in low state for a long time and upper switch closes at time t=0 and lower switch opens just prior to t=0



0V is the initial condition on C_L

Example (cont)

With improved model $t_{LH}=?$

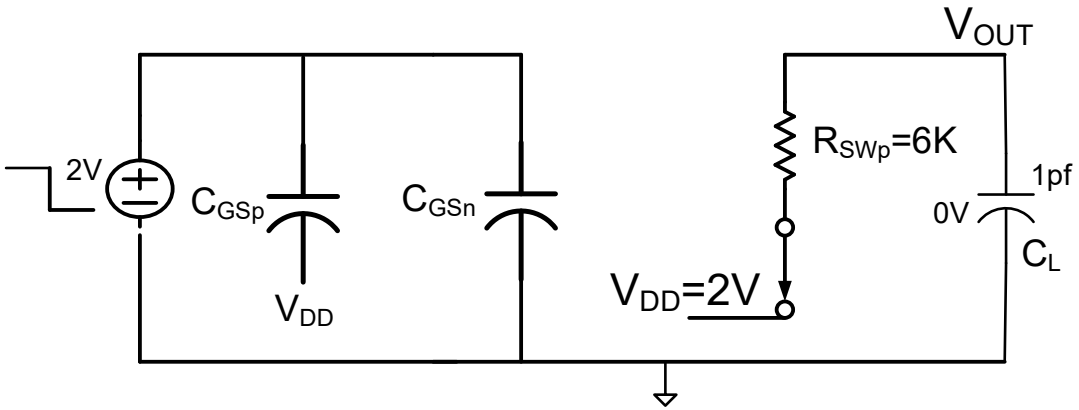


$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

For this circuit (specifically on the right), F=2, I=0 and $\tau = R_{SWp}C_L$

Example (cont)

With improved model

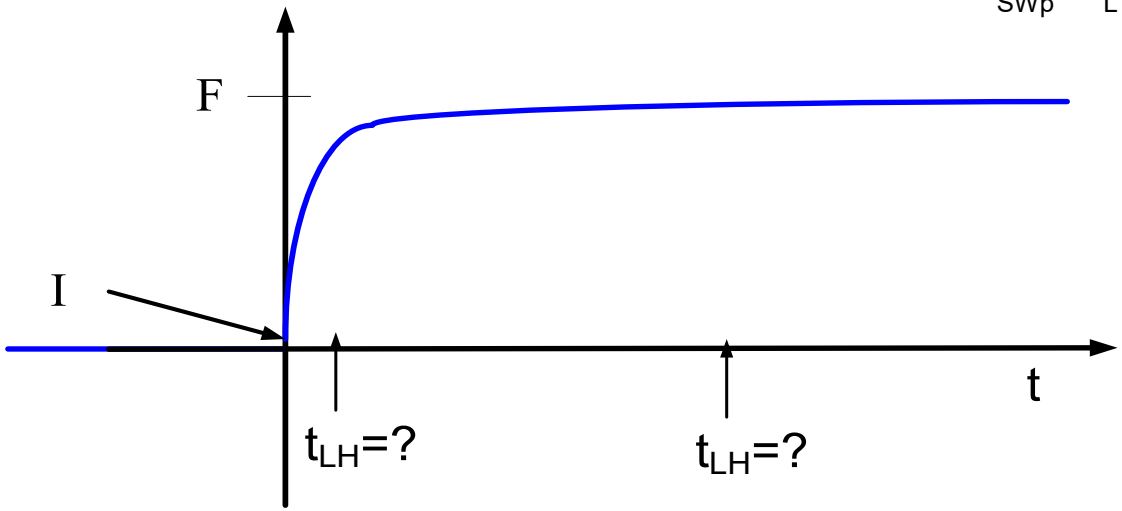


$$t_{LH}=?$$

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 2\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\tau = R_{SWp}C_L$$

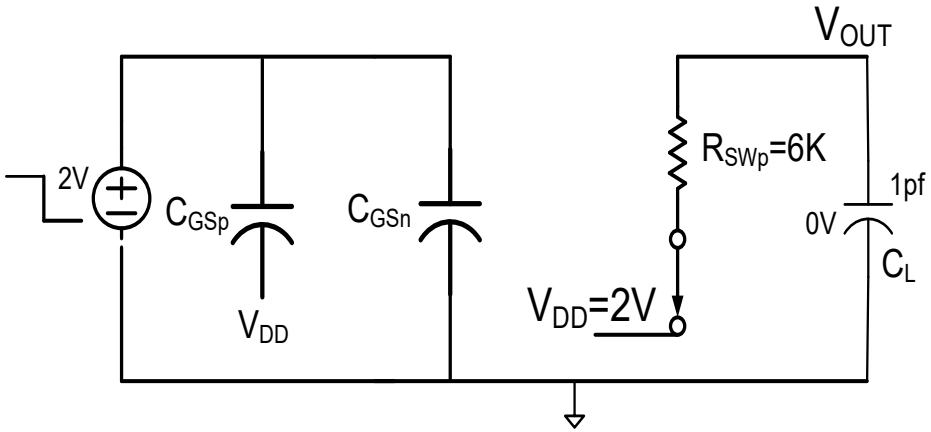


how is t_{LH} defined?

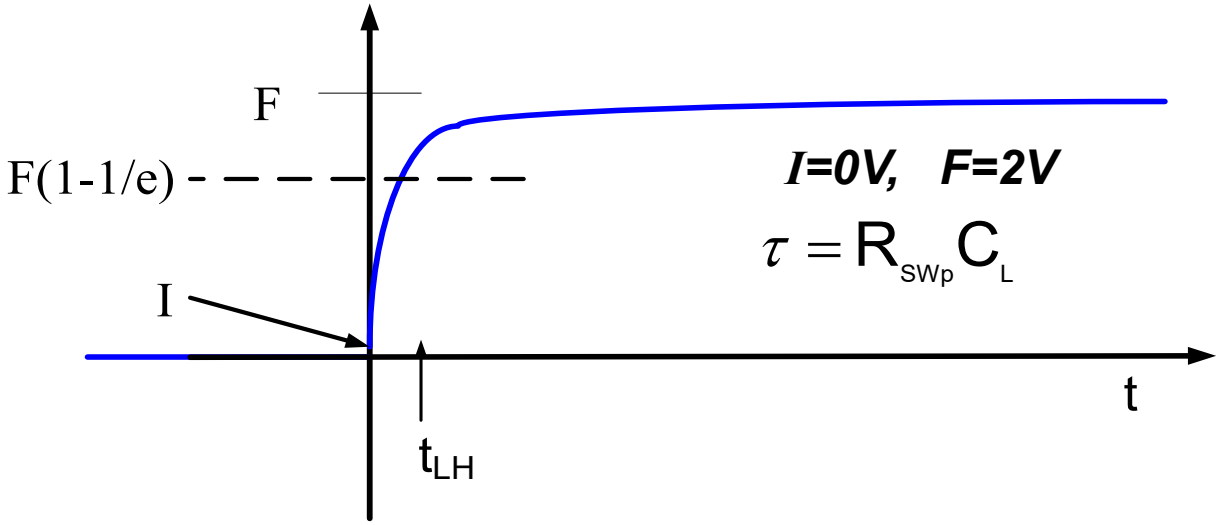
Example (cont)

With improved model

t_{LH}=?



Define t_{LH} as shown on figure



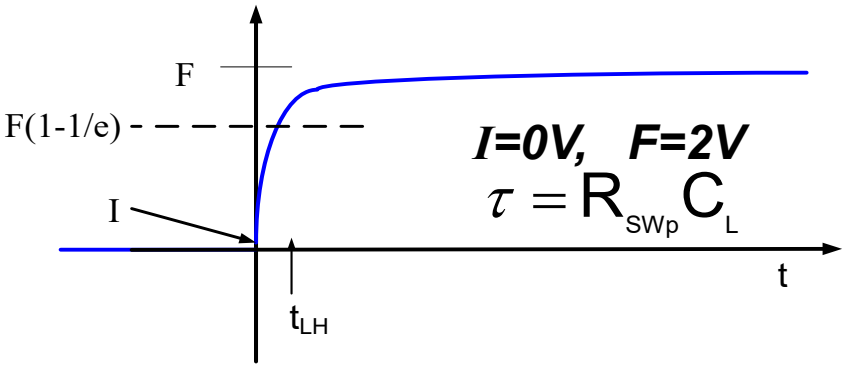
t_{LH} as defined has proven useful for analytically predicting response time of circuits

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Rightarrow \quad F\left(1 - \frac{1}{e}\right) = F + (I - F)e^{-\frac{t_{LH}}{\tau}}$$

Example (cont)

With improved model

t_{LH}=?



$$F\left(1-\frac{1}{e}\right)=F+\left(I-F\right)e^{-\frac{t_{LH}}{\tau}}$$

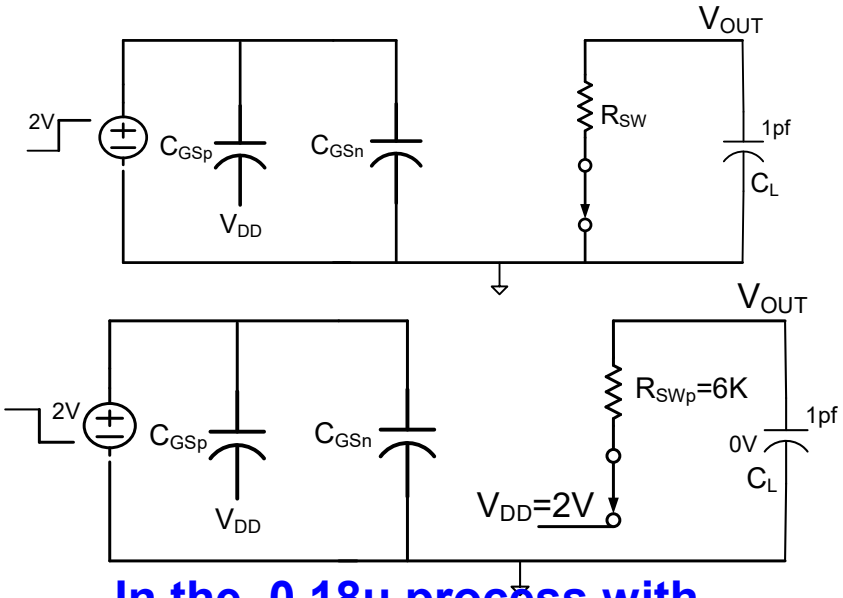
$$F\left(1-\frac{1}{e}\right)=F+\left(F\right)e^{-\frac{t_{LH}}{\tau}}$$

$$1-\frac{1}{e}=1+e^{-\frac{t_{LH}}{\tau}}$$

$$t_{LH}=\tau \quad \Rightarrow \quad t_{LH}=R_{SWp}C_L$$

Example (cont)

With improved model



In the 0.18u process with minimum-sized devices

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

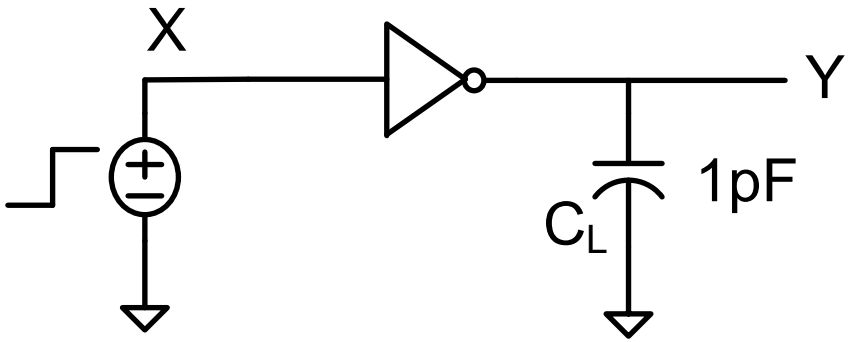
$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Note this circuit is quite fast !

Note that t_{HL} is much shorter than t_{LH}

Often C_L will be even smaller and the circuit will be much faster !!

Summary: What is the delay of a minimum-sized inverter driving a 1pF load?

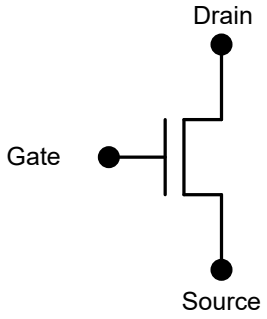


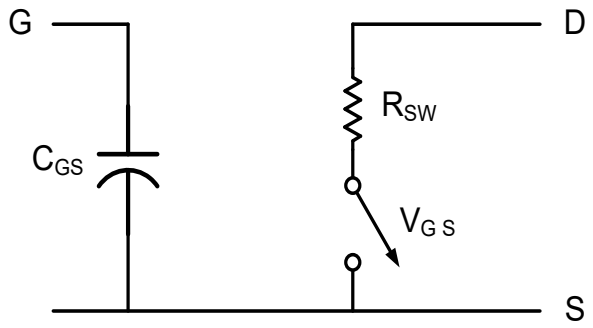
In a 0.18µ process

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Improved switch-level model





Switch closed for V_{GS}= large

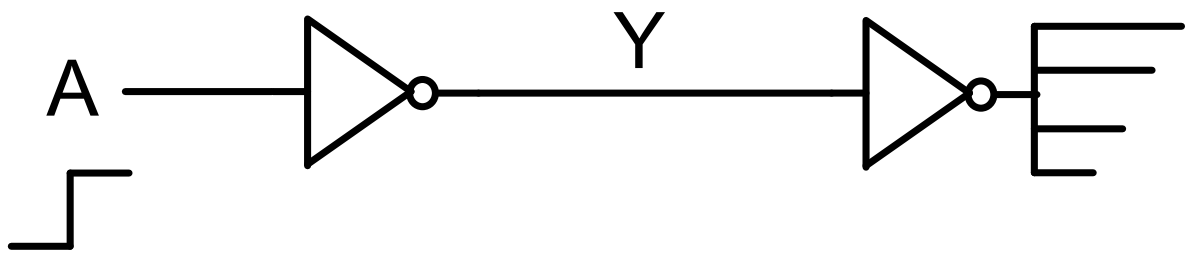
Switch open for V_{GS}= small

- **Previous example showed why R_{SW} in the model was important**
- **But of what use is the C_{GS} which did not enter the previous calculations?**

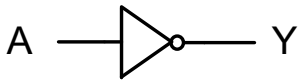
For minimum-sized devices in a 0.18μ process

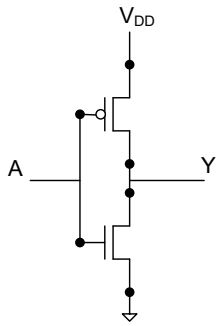
$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{cases}$$

One gate often drives one or more other gates !

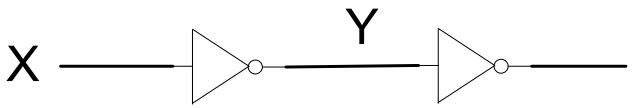


What are t_{HL} and t_{LH}?



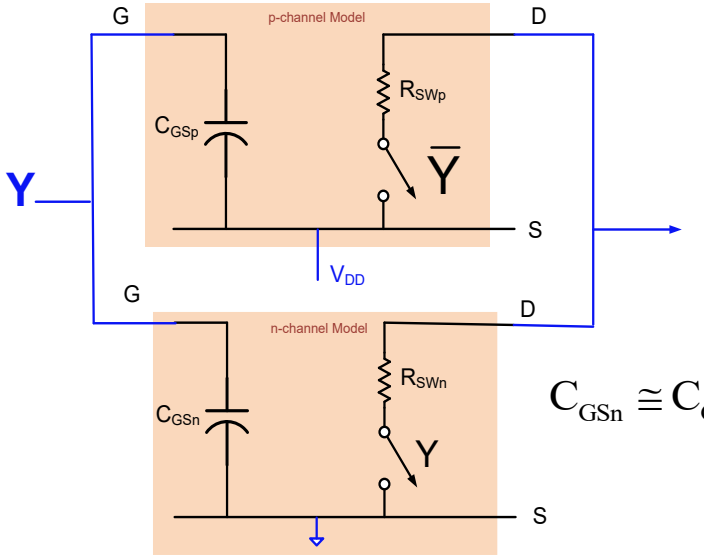


Example: What is the delay of a minimum-sized inverter driving another identical device?



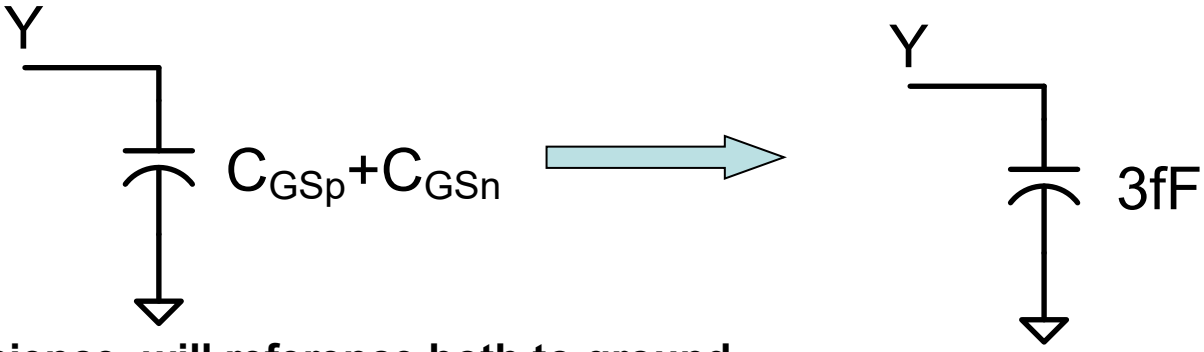
Load on first inverter

C_{GSn} and C_{GSp} both 1.5fF



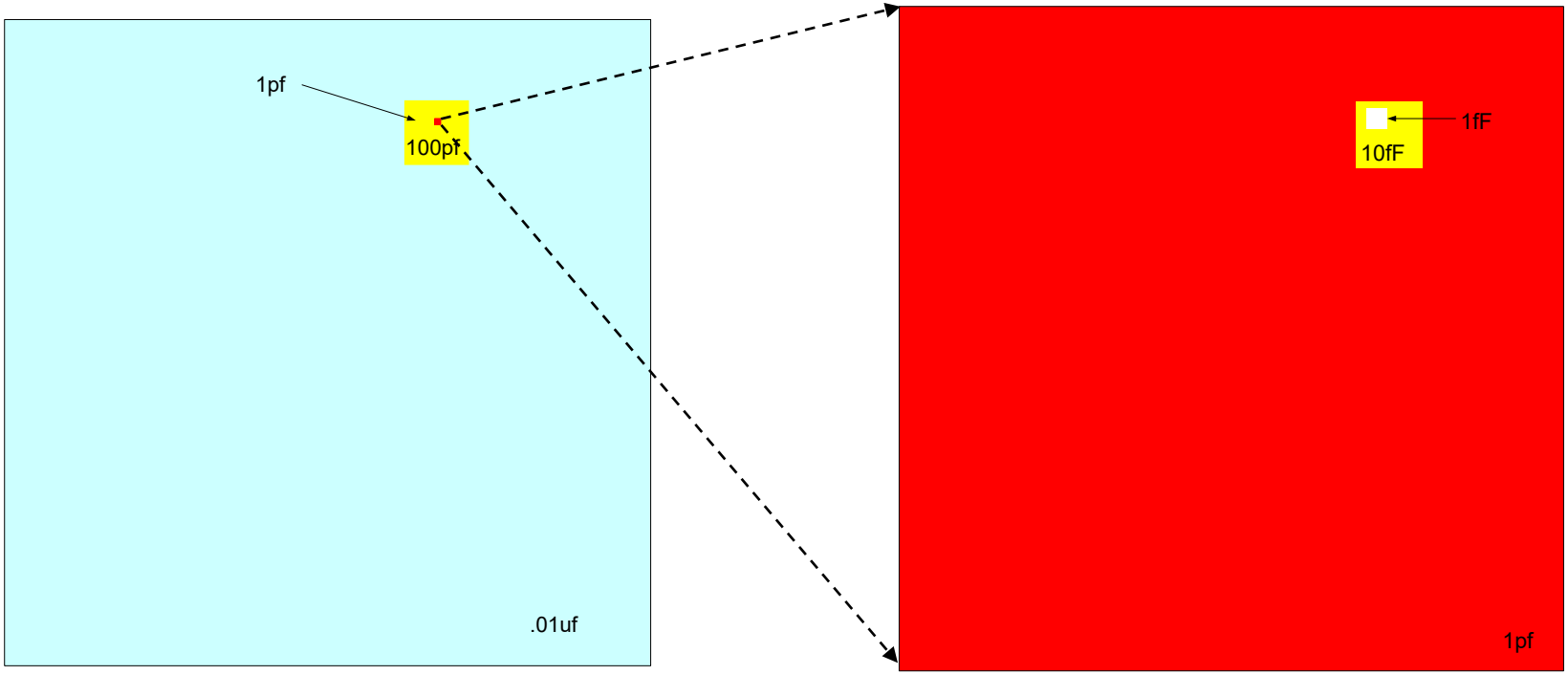
$C_{GSn} \cong C_{GSp} \cong 1.5\text{fF}$

Loading effects same whether C_{GSp} and/or C_{GSn} connected to V_{DD} or GND



For convenience, will reference both to ground

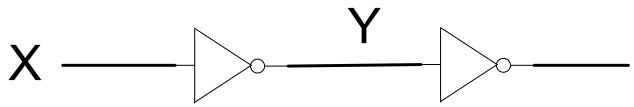
Is a capacitor of 1.5fF small enough to be neglected?

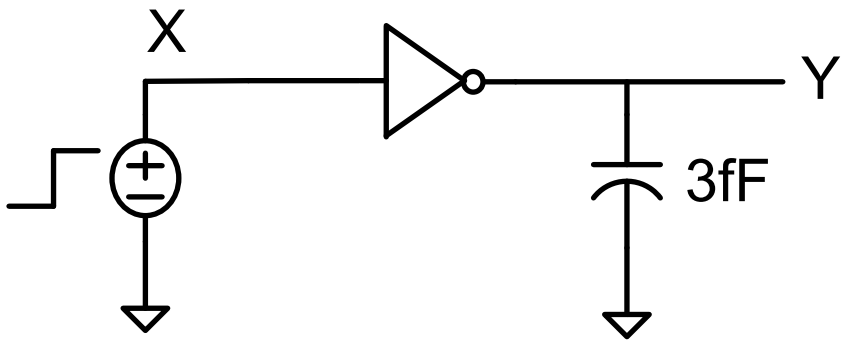


Area allocations shown to relative scale:

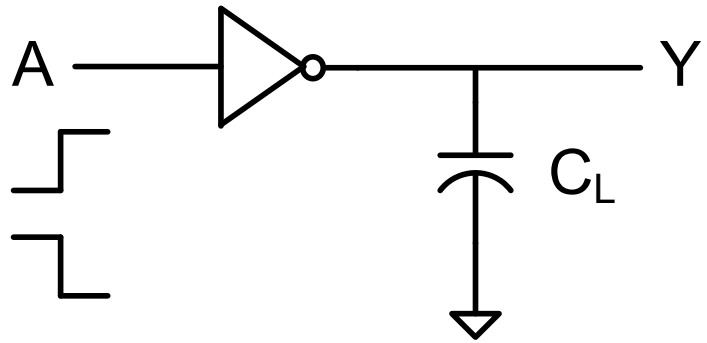
- **This example will provide insight into the answer of the question**

Example: What is the delay of a minimum-sized inverter driving another identical device? Assume V_{DD}=2V





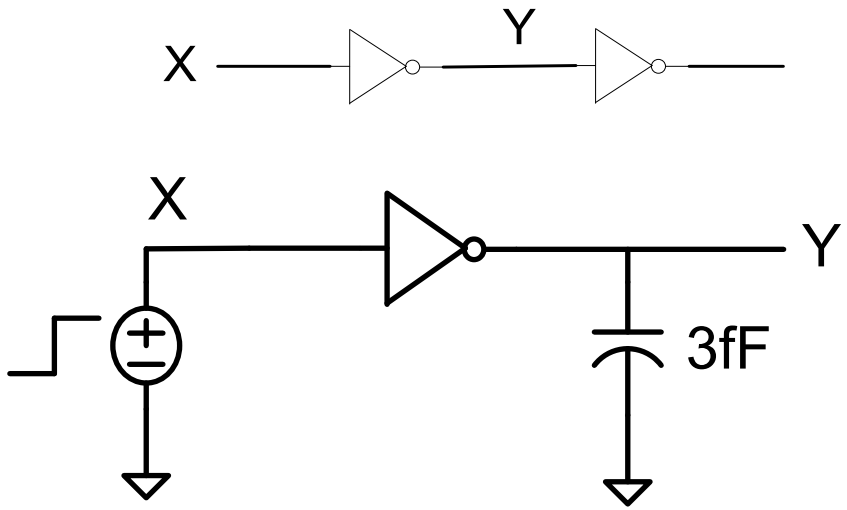
Generalizing the Previous Analysis to Arbitrary Load



$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

Example: What is the delay of a minimum-sized inverter driving another identical device?



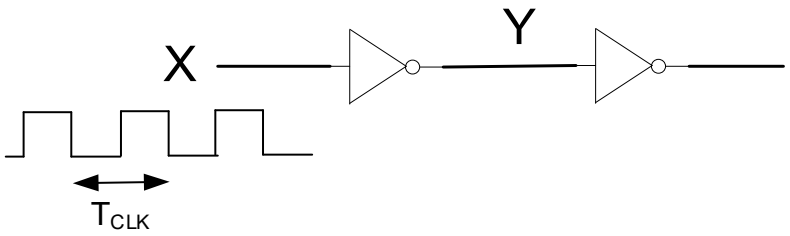
$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 3\,fF = 6\,p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 3\,fF = 18\,p\,\text{sec}$$

Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?

Example: What is the delay of a minimum-sized inverter driving another identical device?



$$t_{HL} \cong R_{SWn} C_L = 6p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 18p\,\text{sec}$$

What would be the maximum clock rate for acceptable operation?

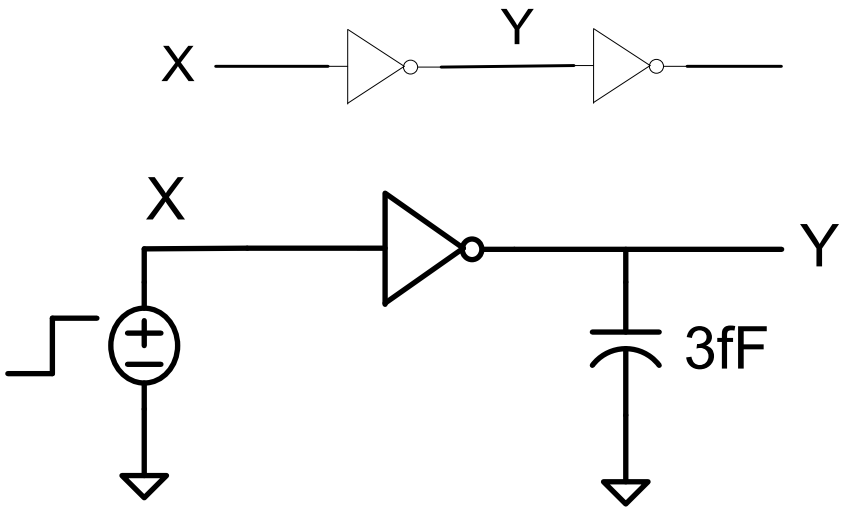
$$T_{CLK\text{-}min} = t_{HL} + t_{LH}$$

$$f_{CLK\text{-}max} = \frac{1}{T_{CLK\text{-}min}} = \frac{1}{24\text{psec}} = 40\text{GHz}$$

And much faster in a finer feature process !! **??????**

What would be the implications of allowing for 10 levels of logic and 10 loads (FanOut=10)?

Example: What is the delay of a minimum-sized inverter driving another identical device? SUMMARY



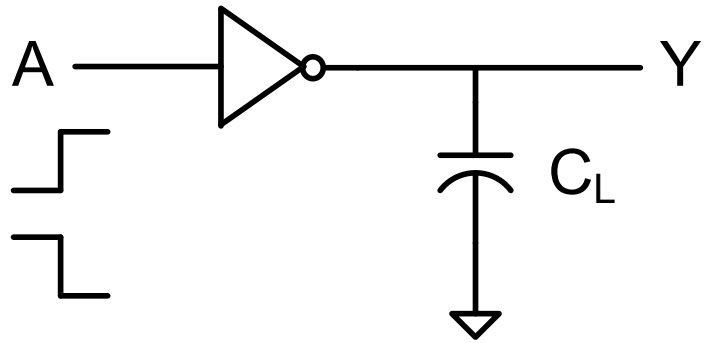
$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 3\,fF = 6\,p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 3\,fF = 18\,p\,\text{sec}$$

This is very fast but even the small 1.5fF capacitors are not negligible !

These capacitors play a key role in determining the speed of a circuit !

Response time of logic gates



$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

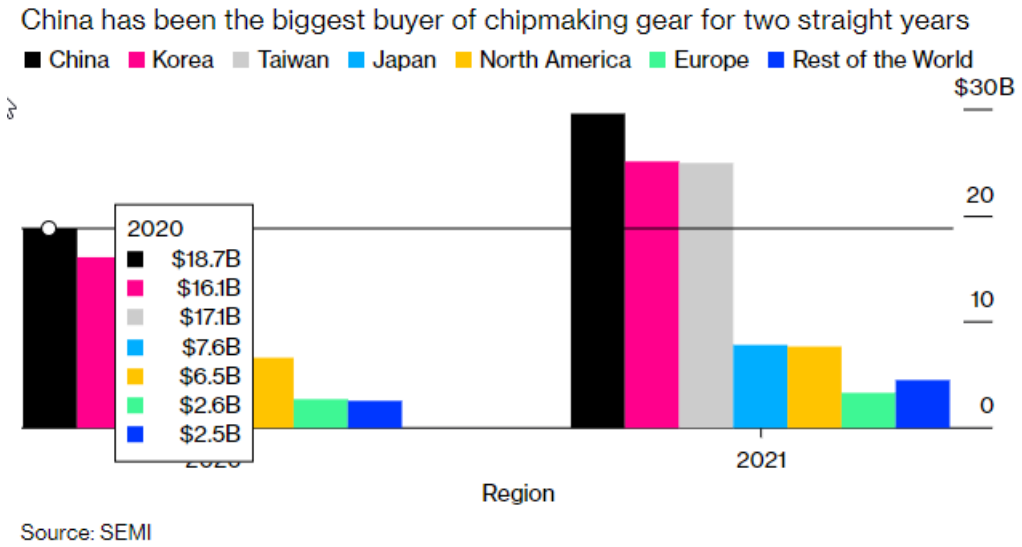
- **Logic Circuits can operate very fast**
- **Extremely small parasitic capacitances play key role in speed of a circuit**

Some Observations about Technology and Politics

Are the larger feature size technologies still used by industry today in the US or abroad?

GlobalData predicts that the Chinese market will play a much smaller role for foreign suppliers by 2030. More than 90% of the chips sold and used worldwide involve low-process production technology.

https://www.investmentmonitor.ai/analysis/china-lead-global-semiconductor-growth 2030#:~:text=Global%20semiconductor%20industry%20revolves%20around,Samsung 20Electronics%20and%20SK%20Hynix.



Some Observations about Technology and Politics

Sept 2022

https://technode.com/2021/03/04/where-china-is-investing-in-semiconductors-in-charts/

China is the world's largest consumer of semiconductors, and the lion's share of revenue from purchasing these chips go to foreign firms. China consumed $143.4 billion worth of wafers in 2020, and just 5.9% of them were produced by companies headquartered in China.

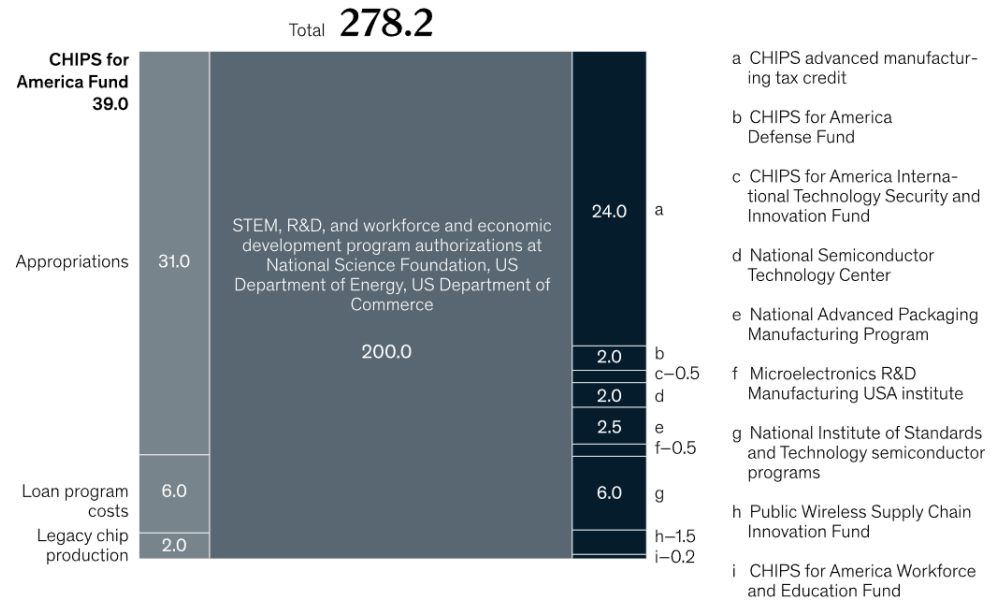
The Chips Act of 2022

$52 billion grant over five years to help grow the domestic semiconductor manufacturing. $2 billion of which is to explicitly focus on legacy chip production. These chips are essential to the auto industry, the military, and other industries critical to our national security interests.

By the numbers: The CHIPS Act directs $280 billion in spending over the next ten years. The majority—$200 billion—is for scientific R&D and commercialization. Some $52.7 billion is for semiconductor manufacturing, R&D, and workforce development, with another $24 billion worth of tax credits for chip production. There is $3 billion slated for programs aimed at leading-edge technology and wireless supply chains.

The CHIPS and Science Act of 2022 directs $280 billion in spending over the next ten years, with the bulk for scientific R&D.

CHIPS and Science Act funding for 2022–26, $ billion



Source: Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act of 2022, H.R. 4346, 117th Cong. (2022)

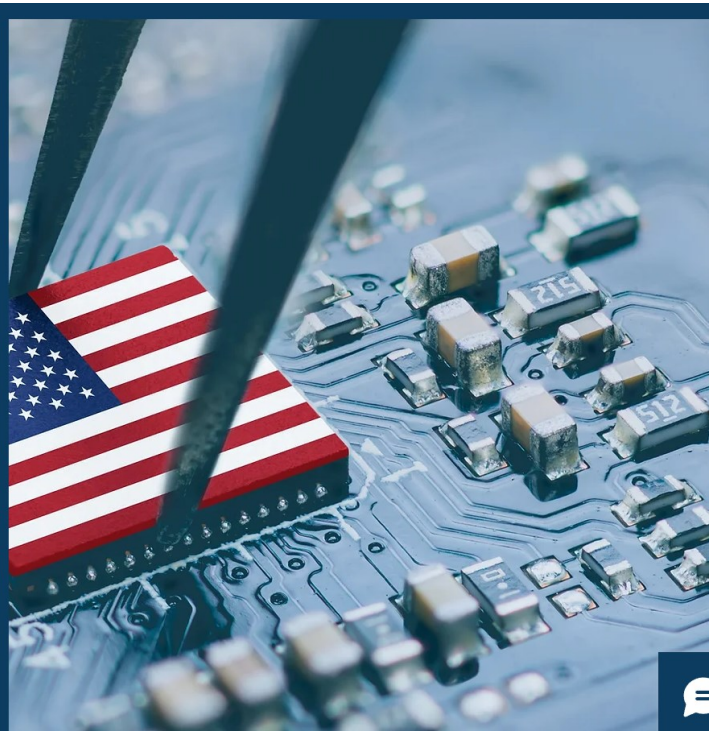
McKinsey & Company

How do I get CHIPS Act Funding?

Breaking News: The application for wafer manufacturers and suppliers of materials and equipment (e.g., chemicals and tools) was just released. Read the details here.

$53 billion is available for semiconductor manufacturing and R&D, plus a 25% refundable tax credit for qualified CapEx. See below to discover where your business fits in

Need help? Book an appointment with our professional grant writing team here or email us: equity@chipsact.com



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2023

Stay Safe and Stay Healthy !

End of Lecture 7